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10/561,135	04/25/2006	Martin Vorbach	2885/98	9404

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EXAMINER	
ALROBAYE, IDRISS N	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/561,135	VORBACH ET AL.	
	Examiner	Art Unit	
	IDRISS N. ALROBAYE	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 12-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 12-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 May 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This action is responsive to amendments received on 9/29/2009.

2. Claims 1-7 and 12-30 still presented for examination. Claims 8-11 cancelled.

3. Applicant's amendments to claims to overcome 35 USC 112 rejections have been considered and several rejections have been withdrawn.

4. Note, Applicant's Remarks title III refers to rejections under 35 USC 112, it's assumed that applicant's meant 35 USC 102 instead of 112 since the arguments refers to 102 rejections.

Continued Examination Under 37 CFR 1.114

5. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9/29/2009 has been entered.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 2-4 and 6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. As per claims 2 and 6, the term "strictly" in the claims is a relative term which renders the claim indefinite. The term "strictly" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1-7 and 12-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dawes U.S. Patent No. 4,967,340 (hereinafter Dawes) in view of Lin U.S. Patent No. 7,043,416 (hereinafter Lin).

11. As per claim 1, Dawes teaches a method of processing data comprising the step of:

coupling:

(a) at least one unit adapted for processing data in a sequential manner (see Dawes, Fig. 2, element 48); and

(b) an array adapted for processing data, the array comprising a plurality of data processing cells that are configurable in their function and the array comprising a configurable network (see Dawes, Fig. 2, elements 28, 50 and abstract);

wherein:

the at least one unit is operable independently of the array (see Dawes, Fig. 2, element 48, which operates independent of the array processor element 28); and

the array is:

at least one of coarse grained and runtime reconfigurable (see Dawes, abstract and col. 1, line 65 to col. 2, line 12);

With regards to the instruction pipeline, although one of ordinary skill in the art at the time of the invention was made would understand that element 48 of Dawes comprises an instruction pipeline for processing instructions. It's common that modern processors have instruction pipelines in order to increase throughput. Applicant's indicated this in the specification as well, that RISC cores employ instruction pipelines to maximize throughput.

However, since Dawes was not explicit on the instruction pipelining, the examiner introduced a secondary reference (Lin) that explicitly shows a processor (CPU) comprising an instruction pipeline (see Lin, Fig. 3 and col. 4, lines 62-67), for the

purpose of maximizing throughput and increasing speed (see Lin, col. 4, lines 62-67 and col. 1, lines 2-41).

Thus, since it would have been obvious to one of ordinary skill in the relevant art to have a pipeline in the CPU (element 48) of Dawes, the array would be coupled to the instruction pipeline since it's coupled to the CPU (element 48) (see also Dawes, Fig. 2, wherein element 48 is coupled to element 28 "array processor").

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of Lin in the invention of Dawes, for the purpose of enhancing speed and increasing throughput thus significantly improving performances.

12. As per claim 2, Dawes further teaches a method according to claim 1, further comprising the step of:

transferring via at least one data path at least one of the an input data and an output data from the at least one unit to the array and from the array to the at least one unit (see Dawes, Fig. 2, wherein elements 28 and 50 communicate with element 48), the at least one data path being provided therebetween and comprising at least one FIFO so as to allow for at least one of (i) a coupling between the at least one unit and the array that is not strictly synchronous and (ii) a data processing within the at least one unit and the array that is not strictly synchronous (see Dawes, abstract and col. 5, lines 27-64; see also Fig. 2, element 34, wherein the RAM is considered to be a FIFO

since it receives data to be stored and send them based on receive time; see also Col. 5, lines 1-24).

13. As per claim 3, Dawes further teaches a method according to claim 2, wherein the transferring is performed by at least one of inserting data directly into and extracting data directly from a data path of at least one of the at least one unit and the array (see Dawes, col. 5, lines 40-64).

14. As per claim 4, Dawes further teaches a method according to claim 3, further comprising the step of:

providing between the at least one unit and the array a path adapted for transfer of at least one of status information and event information (see Dawes, col. 5, lines 40-64; see also Fig. 2, communications between element 48 and 28).

15. As per claim 5, Dawes further teach a device for processing data comprising:

at least one unit adapted for processing data in a sequential manner (see Dawes, Fig. 2, element 48); and

an array adapted for processing data comprising a configurable network and a plurality of data processing cells that are configurable in their function (see Dawes, Fig. 2, elements 28, 50 and abstract);

wherein:

the array is coupled to the instruction pipeline (see Dawes, Fig. 2, wherein element 48 is coupled into element 28 “array processor”; For the pipeline, see Lin as explained below), the coupling of the array to the instruction pipeline including controlling configurations by the instruction pipeline (see Dawes, Fig. 2, and abstract, wherein the CPU element 48 controls the configuration); and

the at least one unit is operable independently of the array (see Dawes, Fig. 2, element 48, which operates independent of the array processor element 28);

With regards to the instruction pipeline, although one of ordinary skill in the art at the time of the invention was made would understand that element 48 of Dawes comprises an instruction pipeline for processing instructions. It’s common that modern processors have instruction pipelines in order to increase throughput. Applicant’s indicated this in the specification as well, wherein RISC cores employ instruction pipelines to maximize throughput.

However, since Dawes was not explicit on the instruction pipelining, the examiner introduced a secondary reference (Lin) that explicitly shows a processor comprising an instruction pipeline (see Lin, Fig. 3 and col. 4, lines 62-67), for the purpose of maximizing throughput and increasing speed (see Lin, col. 4, lines 62-67 and col. 1, lines 2-41).

Thus, since it would have been obvious to one of ordinary skill in the relevant art to have a pipeline in the CPU (element 48) of Dawes, the array would be coupled to the instruction pipeline since it's coupled to the CPU (element 48) (see also Dawes, Fig. 2, wherein element 48 is coupled to element 28 "array processor").

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of Lin in the invention of Dawes, for the purpose of enhancing speed and increasing throughput thus significantly improving performances.

16. As per claim 6, Dawes further teaches the device according to claim 5, wherein at least one of:

at least one data path is provided between the array and the at least one unit, the at least one data path comprising at least one FIFO that allows at least one of (i) a coupling between the at least one unit and the array that is not strictly synchronous and (ii) a data processing within the at least one unit and the array that is not strictly synchronous (see Dawes, abstract and col. 5, lines 27-64; see also rejection of claim 2 for more details); and

data is transferred by at least one of extracting data directly from and inserting data directly into a data path of at least one of the at least one unit and the array (see Dawes, col. 5, lines 40-64).

17. As per claim 7, Dawes teaches a method of processing data comprising the steps of:

coupling:

(a) at least one unit adapted for processing data in a sequential manner (see Dawes, Fig. 2, element 48); and

(b) an array adapted for processing data, the array comprising a plurality of data processing cells that are configurable in their function and a configurable network (see Dawes, Fig. 2, elements 28, 50 and abstract); and

providing a path allowing for block data transfer from the array and at least one of a data cache and another data source (see Dawes, abstract and col. 2, lines 2-31);

With regards to the instruction pipeline, although one of ordinary skill in the art at the time of the invention was made would understand that element 48 of Dawes comprises an instruction pipeline for processing instructions. It's common that modern processors have instruction pipelines in order to increase throughput. Applicant's indicated this in the specification as well, wherein RISC cores employ instruction pipelines to maximize throughput.

However, since Dawes was not explicit on the instruction pipelining, the examiner introduced a secondary reference (Lin) that explicitly shows a processor comprising an instruction pipeline (see Lin, Fig. 3 and col. 4, lines 62-67), for the purpose of maximizing throughput and increasing speed (see Lin, col. 4, lines 62-67 and col. 1, lines 2-41).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of Lin in the invention of Dawes, for the purpose of enhancing speed and increasing throughput thus significantly improving performances.

18. As per claim 12, Dawes further teaches a method according to claim 1, wherein the at least one unit includes at least one of a CPU, a von-Neumann-Processor, and a microcontroller (see Dawes, Fig. 2, element 48).

19. As per claim 13, Dawes further teaches a method according to claim 1, wherein the array includes at least one of a data processor, a Field Programmable Gate-Array (FPGA), a Data Flow Processor (DFP), a Digital Signal Processor (DSP), an eXtreme Processing Platform (XPP), and a chaemeleon-technology data processing fabric (see abstract and Fig. 2, elements 28 and 50).

20. As per claim 14, Dawes further teaches a method according to claim 2, wherein the at least one data path between the at least one unit and the array includes at least one local memory connected to the at least one unit as a cache and connected to the array (see Fig. 2 and col. 2, lines 2-45).

21. As per claim 15, Dawes further teaches a method according to claim 14, wherein the at least one local memory includes an internal RAM (IRAM) (see col. 2, lines 12-24).

22. As per claim 16, Dawes and Lin further teach a method according to claim 1, wherein configuration information for the array is issued by the instruction pipeline of the at least one unit (see abstract and col. 5, lines 27-64; For the pipeline, see Lin as explained in claim 1).

23. As per claim 17, Dawes further teaches a method according to claim 16, further comprising:

buffering the configuration information in at least one FIFO so as to allow for at least one of a coupling between and a data processing within the at least one unit and the array that is not strictly synchronous (see col. 5, lines 27-64).

24. As per claim 18, Dawes further teaches a method according to claim 1, wherein the at least one unit supports multi-threading, and the array is connected as a thread unit (see col. 5, lines 27-64).

25. As per claim 19, Dawes further teaches a method according to claim 18, wherein the array is operable synchronously to the unit (see abstract and col. 5, lines 27-64).

26. As per claim 20, Dawes further teaches a method according to claim 4, wherein the at least one of the status information and the event information includes at least one of flags, an overflow, and a carry (see col. 2, lines 1-61).

27. As per claim 21, Dawes further teaches a device according to claim 5, wherein the at least one unit includes at least one of a CPU, a von-Neumann-Processor, and a microcontroller (see Fig. 2, element 48).

28. As per claim 22, Dawes further teaches a device according to claim 5, wherein the array includes a runtime and reconfigurable data processor (see abstract and col. 2, lines 2-24).

29. As per claim 23, Dawes further teaches a device according to claim 6, wherein the at least one data path includes at least one local memory connected to the unit as cache and connected to the array (see abstract and col. 5, lines 27-64).

30. As per claim 24, Dawes further teaches a method according to claim 23, wherein the at least one local memory includes an internal RAM (IRAM) (see col. 2, lines 12-24).

31. As per claim 25, Dawes and Lin further teach a device according to claim 5, wherein configuration information for the array is issued by the instruction pipeline (see Dawes, abstract and col. 5, lines 27-64; For the pipeline, see Lin as explained in claim 1).

32. As per claim 26, Dawes further teaches a device according to claim 25, wherein the configuration information is buffered in at least one FIFO so as to allow for at least one of (i) a coupling between the at least one unit and the array that is not strictly synchronous and (ii) a data processing within the at least one unit and the array that is not strictly synchronous (see Dawes, abstract and col. 5, lines 27-64; see rejection of claim 2 for more details).

33. As per claim 27, Dawes further teaches a device according to claim 5, wherein the at least one unit supports multi-threading, and the array is connected as a thread unit (see col. 5, lines 27-64).

34. As per claim 28, Dawes further teaches a device according to claim 27, wherein the array operates synchronously to the unit (see abstract and col. 5, lines 27-64).

35. As per claim 29, Dawes further teaches a method according to claim 7, wherein the at least one unit includes at least one of a CPU, a von-Neumann-processor, and a microcontroller (Fig. 2, element 48 and abstract).

36. As per claim 30, Dawes further teaches a method according to claim 7, wherein the array includes at least one of a runtime and reconfigurable data processor, a Data Flow Processor (DFP), a Digital Signal Processor (DSP), an eXtreme Processing Platform (XPP), and a chaemeleon-technology data processing fabric (see abstract and Fig. 2, elements 28 and 50).

Response to Arguments

37. Applicant's arguments filed 9/29/2009 have been fully considered but they are not persuasive.

38. **Applicant's Argument**:

"*The Office Action refers generally to an asserted coupling between elements 48 and 28 of the Dawes reference as asserted disclosing the coupling of the array to the instruction pipeline. However, while the Dawes reference indicates that a CPU 48 and compiler 46 may form a configuration controller for configuring the random access processor 28, the Dawes reference makes no reference to an instruction pipeline, and certainly does not disclose, or even suggest, that the random access processor 28 may be coupled to an instruction pipeline of the CPU 48. The mere transmittal of instructions does not disclose an instruction pipeline.*"

Examiner's Response:

The examiner respectfully disagrees. With regards to the instruction pipeline, although one of ordinary skill in the art at the time of the invention was made would understand that element 48 of Dawes comprises an instruction pipeline for processing instructions. It's common that modern processors have instruction pipelines in order to increase throughput. Applicant's indicated this in the specification as well, wherein RISC cores employ instruction pipelines to maximize throughput.

However, since Dawes was not explicit on the instruction pipelining, the examiner introduced a secondary reference (Lin) that explicitly shows a processor comprising an instruction pipeline (see Lin, Fig. 3 and col. 4, lines 62-67), for the purpose of maximizing throughput and increasing speed (see Lin, col. 4, lines 62-67 and col. 1, lines 2-41).

Thus, since it would have been obvious to one of ordinary skill in the relevant art to have a pipeline in the CPU (element 48) of Dawes, the array would be coupled to the instruction pipeline since it's coupled to the CPU (element 48) (see also Dawes, Fig. 2, wherein element 48 is coupled to element 28 "array processor").

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of Lin in the invention of Dawes, for the purpose of enhancing speed and increasing throughput thus significantly improving performances.

39. **Applicant's Argument**:

"As further regards claim 2, claim 2 provides that at least one data path is provided between the array and the at least one unit and includes a FIFO. The Office Action refers to the Abstract and column 5, lines 27 to 64 of the Dawes reference as asserted disclosing this feature. However, the cited sections do not refer to memory of any kind between the CPU 48 and the random access processor 28 (referred to by the Office Action as asserted disclosing the at least one unit and the array, respectively), let alone a FIFO. Indeed, any review of the Dawes reference makes plain that it does not at all disclose, or even suggest, a FIFO.

Moreover, claim 2 has been amended herein without prejudice to clarify the transferring step to include a transfer from the at least one unit to the array and vice versa. In contrast to claim 2, the Dawes reference provides for processing to be performed only by the random access processor 28. The CPU 48 is used merely to configure the random access processor 28. No data is indicated to be transferred from the random access processor 28 to the CPU 48."

Examiner's Response:

The examiner respectfully disagrees. As shown in col. 5, lines 1-26 of Dawes, the multiport RAM acts as a signal path bus which is considered equivalent to FIFO since the multiport receives and send data. Furthermore, the multiport RAM also stores data which is also similar to a FIFO since it stores data as well. Furthermore, Dawes, Fig. 2, element 28 and 50 communicate with element 48, wherein the CPU as explained, have an instruction pipeline communicate with the array elements 28 and 50, and thus reads on current claim language.

Conclusion

40. Any inquiry concerning this communication or earlier communications from the examiner should be directed to IDRISS N. ALROBAYE whose telephone number is (571)270-1023. The examiner can normally be reached on Mon-Fri from 8:00 to 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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